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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/615,503 | 07/13/2000 | NOBUAKI HASHIMOTO | 101929.02 | 3462 |

7590 01/24/2002

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| EXAMINER | |
|---|---|
| COLLINS, DEVEN M | |
| ART UNIT | PAPER NUMBER |
| 2823 | |

DATE MAILED: 01/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/615,503 | HASHIMOTO, NOBUAKI | |
| | Examiner | Art Unit | |
| | D. M. Collins | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restriction*

1. Applicant's election with traverse of claims 1-17 in Paper No. 7 was acknowledged. The traversal was on the ground(s) that the Examiner has not properly pointed out why the two inventions could not be considered together. This is not found persuasive because the area of search for claims 18-20 is not under the Examiner's classification area.

However, upon applicant's request for reconsideration, Examiner rejoins claims 18-20 because of their dependence on claim 1.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,057,174. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of application 09/615,503 show a method for fabricating a device. Similarly, from U.S. Patent No.6,057,174, a semiconductor device, a method for fabricating, and an electronic apparatus is shown. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide fabrication of microelectronic circuit components to improve microminiaturization of semiconductor devices.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being unpatentable over Hur (6,033,933, dated 3/7/00).

Hur shows the method as claimed in the Figures 1-6 with corresponding text. In re claim 1, Hur discloses a method of fabricating a semiconductor device 6 comprising:

a step (a) of attaching a plurality of semiconductor chips 1 to a tape;

a step (b) of cutting the tape 11; and

a step (c) of providing a plurality of external terminals 3 on a substrate Fig. 3 cut from the tape in the step (b), wherein the steps (a) and (b) are carried out in a reel-to-reel transport system (col. 3, par. 8).

In re claim 2, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, further comprising:

a step of adhering a reinforcing member to the tape 11 in positions corresponding to each of the semiconductor chips 1, before the step (b).

In re claim 3, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, wherein the tape 11 is cut into regions each including one of the semiconductor chips 1 in the step (b).

In re claim 4, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 2, wherein the tape 11 is cut into regions each including one of the semiconductor chips 1 in the step (b).

In re claim 5, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, wherein the tape 11 is cut into regions each including two or more of the semiconductor chips 1 in the step (b).

In re claim 6, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 2, wherein the tape 11 is cut into regions each including two or more of the semiconductor chips 1 in the step (b).

In re claim 7, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 5, wherein the substrate cut from the tape 11 is further cut into the semiconductor chips 1 after the step (c).

In re claim 8, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 6, wherein the substrate cut from the tape 11 is further cut into the semiconductor chips 1 after the step (c).

In re claim 9, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, wherein a plurality of device holes 10 are formed in the tape 11, and leads are formed above the tape 11, whose end portions project into the respective device holes 10;
and wherein each of the semiconductor chips 1 is disposed within a respective of the device holes 10, and the electrodes 3 of the semiconductor chips 1 and the leads are bonded in the step (a) .

In re claim 10, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, wherein each of the semiconductor chips 1 is bonded to the tape 11 in a face-down configuration in the step (a).

In re claim 11, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 10, wherein by means of an anisotropic conductive material, the electrodes 3 of the semiconductor chips 1 and leads formed above the tape 11 are electrically connected in the step (a).

In re claim 12, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, wherein each of the semiconductor chips 1 is bonded to the tape 11 in a face-up configuration in the step (a).

In re claim 13, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 12, wherein the electrodes 3 of the semiconductor chips 1 and leads formed above the tape 11 are electrically connected by means of wires 4 in the step (a) .

In re claim 14, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 1, further comprising:

a step of adhering a heat radiating member to each of the semiconductor chips 1.

In re claim 15, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 2, further comprising:

a step of adhering a heat radiating member to each of the semiconductor chips 1.

In re claim 16, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 14, wherein the step of adhering the heat radiating member is carried out before the step (b), with a reel-to-reel transport system (col. 3, par. 8).

In re claim 17, Hur discloses the method of fabricating a semiconductor device 6 as defined in claim 15,

wherein the step of adhering the heat radiating member is carried out before the step (b), with a reel-to-reel transport system (col. 3, par. 8).

In re claim 18, Hur discloses a semiconductor device 6 fabricated by the method as defined in claim 1.

In re claim 19, Hur discloses a circuit board (fig. 3) having mounted the semiconductor device 6 as defined in claim 18.

In re claim 20, Hur discloses an electronic apparatus (fig. 3) including the semiconductor device 6 as defined in claim 18.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Deven M. Collins whose telephone number is (703) 305-7840. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DMC

January 11, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800